REMARKS

In the non-final Office Action, the Examiner rejected claims 15 and 28 under 35 U.S.C. § 102(b) as anticipated by Wang (U.S. Patent No. 5,563,891); rejected claims 16-22 under 35 U.S.C. § 103(a) as unpatentable over Wang in view of Serack (U.S. Patent No. 5,111,485); rejected claim 23 under 35 U.S.C. § 103(a) as unpatentable over Wang in view of Serack and Co et al. (U.S. Patent No. 5,602,882); and rejected claims 24-27 under 35 U.S.C. § 103(a) as unpatentable over Wang in view of Serack and Mays et al. (U.S. Patent No. 5,384,770). The Examiner objected to claims 29-36 as dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include the features of the base claim and any intervening claims. The Examiner allowed claims 1-14 and 37-45.

By this Amendment, Applicants cancel claim 18 without prejudice or disclaimer and amend claims 15, 16, and 19-28 to improve form. Applicants appreciate the Examiner's identification of allowable subject matter, but respectfully traverse the Examiner's rejections under 35 U.S.C. §§ 102 and 103 with regard to the claims as amended herein. Claims 1-17 and 19-45 are pending.

In paragraph 3 of the Office Action, the Examiner rejected claims 15 and 28 under 35 U.S.C. § 102(b) as allegedly anticipated by Wang. Applicants respectfully traverse the rejection.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. In other words, the identical invention must be shown in as complete detail as contained in the claim. See M.P.E.P. § 2131. Wang does not disclose or suggest the combination of features recited in amended claims 15 and 28.

Amended claim 15, for example, recites a system for reliably receiving data. The system comprises means for receiving data and an unreliable clock signal; means for writing the data to a memory using the unreliable clock signal; means for generating a reliable clock signal by turning on and off a local clock signal; means for generating a data enable signal; means for reading the data from the memory using the data enable signal and the local clock signal without using the reliable clock signal; and means for recovering the data based on the reliable clock signal.

Wang does not disclose or suggest the combination of features recited in claim 15. For example, Wang does not disclose or suggest means for reading the data from the memory using the data enable signal and the local clock signal and without using the reliable clock signal.

The Examiner alleged that Wang discloses that the data is read out from elastic buffer 620 using the gapped read clock based on the justification signal and the local oscillator signal (Office Action, page 3). Claim 15 now recites, however, means for reading the data from the memory using the data enable signal and the local clock signal and without using the reliable clock signal. As shown in Fig. 3, Wang clearly shows that data is read out of elastic buffer 620 using the gapped read clock, which the Examiner equated to the claimed reliable clock signal (Office Action, page 2).

For at least these reasons, Applicants submit that claim 15 is not anticipated by Wang.

Claim 28 has been amended to recite features of claim 29, which were identified by the Examiner as containing allowable subject matter. Claim 28 is, therefore, not anticipated by Wang and should be in condition for immediate allowance by the Examiner.

In any event, Wang does not disclose or suggest a reliable clock generator that includes first and second state machines, as recited in amended claim 28. Therefore, claim 28 is not anticipated by Wang.

In paragraph 4 of the Office Action, the Examiner rejected claims 16-22 under 35 U.S.C. § 103(a) as allegedly unpatentable over Wang in view of Serack. Applicants respectfully traverse the rejection.

Amended claim 16, for example, recites a method for recovering data that comprises receiving data and an unreliable clock signal; writing the data to a memory using the unreliable clock signal; providing a first state machine to generate a first enable signal and a second enable signal; providing a second state machine to generate a gapped clock signal by turning on and off a constant local clock signal based on the second enable signal; and reading the data from the memory using the first enable signal and the constant local clock signal.

Neither Wang nor Serack, whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 16. For example, neither Wang nor Serack discloses or suggests providing a first state machine to generate a first enable signal and a second enable signal, where the first enable signal is used to read data from a memory and the second enable signal is used to generate a gapped clock signal.

The Examiner admitted that Wang does not disclose state machines, but alleged that Serack discloses state machines 30 and 32 that generate gapped clock and control signals and cited column 6, lines 43-68, and column 7, lines 1-13, of Serack for support

(Office Action, page 4). Applicants submit that Serack does not disclose or suggest that either of state machines 30 or 32 generate a first enable signal and a second enable signal, where the first enable signal is used to read data from a memory and the second enable signal is used to generate a gapped clock signal, as required by claim 16.

At column 6, lines 43-68, Serack discloses:

> The VT1.5 state machine 30 produces from the C1.7 clock signal a first gapped bit clock signal, normally comprising groups each of 8 pulses of the C1.7 clock signal except during the bytes V1, V2, V3, and V4, on a line 48 leading to the blocks 28 and 32. During a stuffing event and consequent pointer adjustment, this first gapped clock signal is modified in that for a negative stuff it is not gapped during the byte V3, and for a positive stuff it is additionally gapped during the data byte which follows the byte V3. The virtual buffer and pointer generator 28 indicates, via lines 50 to the VT1.5 state machine 30 and to the selector 24, the need for and direction of a stuffing event and consequent pointer adjustment, and also provides a pointer value to the selector 24 via lines 52, all as further described below.
>
> The VT1.5 state machine 30 supplies control and timing signals via lines 56, at the times of the bytes V1 to V4, to the virtual buffer and pointer generator 28 and to the selector 24. The virtual buffer and pointer generator 28 is also supplied via a line 58 with a control signal from the multiplier 26, which produces this control signal by frequency multiplying the DS-1 clock signal on the line 38 by a factor of 208/193. It should be appreciated that this factor is the ratio of the number of bits in each 125 μs frame of the VT SPE to the number of bits in each 125 μs frame of the incoming DS-1 signal.

In this section, Serack discloses that state machine 30 generates a gapped clock signal that it sends to state machine 32 and control signals that it supplies to virtual buffer and pointer generator 28. Nowhere in this section, or elsewhere, does Serack disclose or suggest that state machine 30 generates, for example, a first enable signal that is used to read data from a memory, as required by claim 16.

At column 7, lines 1-13, Serack discloses:

> The VT SPE state machine 32 has 104 states which are consecutively cycled through in response to the first gapped clock signal on the line 48, corresponding

> to the 4 frames of 26 bytes in the VT SPE superframe shown in FIG. 1. It gaps the first gapped clock signal on the line 48 with the gapping ratio of 208/193, corresponding to the nature of the 193 DS-1 data bits in the VT SPE frame of 208 bits as shown in FIG. 1, to produce the second gapped bit clock signal on the line 40 as already described. The VT SPE state machine 32 also produces control signals on lines 60 to the selector 24, and a timing signal at the time of the byte V5 on a line 62 to the virtual buffer and pointer generator 28.

In this section, Serack discloses that state machine 32 generates a gapped clock signal that it sends to data buffer 20 and framing logic 22 and control signals that it supplies to selector 24. Nowhere in this section, or elsewhere, does Serack disclose or suggest that state machine 32 generates, for example, a second enable signal that is used by another state machine to generate a gapped clock signal, as required by claim 16.

For at least these reasons, Applicants submit that claim 16 is patentable over Wang and Serack, whether taken alone or in any reasonable combination. Claims 17-22 depend from claim 16 and are, therefore, patentable over Wang and Serack for at least the reasons given with regard to claim 16.

In paragraph 5, the Examiner rejected claim 23 under 35 U.S.C. § 103(a) as allegedly unpatentable over Wang in view of Serack and Co et al. Applicants respectfully traverse the rejection.

Claim 23 depends from claim 16. Without acquiescing in the Examiner's rejection, Applicants submit that the disclosure of Co et al. does not cure the deficiencies in the disclosures of Wang and Serack, as identified above with regard to claim 16. Claim 23 is, therefore, patentable over Wang, Serack, and Co et al., whether taken alone or in any reasonable combination, for at least the reasons given with regard to claim 16.

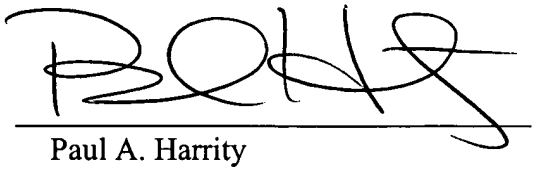
In paragraph 6 of the Office Action, the Examiner rejected claims 24-27 under 35 U.S.C. § 103(a) as allegedly unpatentable over Wang in view of Serack and Mays et al. Applicants respectfully traverse the rejection.

Claims 24-27 depend from claim 16. Without acquiescing in the Examiner's rejection, Applicants submit that the disclosure of Mays et al. does not cure the deficiencies in the disclosures of Wang and Serack, as noted above with regard to claim 16. Claims 24-27 are, therefore, patentable over Wang, Serack, and Mays et al., whether taken alone or in any reasonable combination, for at least the reasons given with regard to claim 16.

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and allowance of pending claims 1-17 and 19-45.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

HARRITY & SNYDER, L.L.P

By: 
Paul A. Harrity
Reg. No. 39,574

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11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
571-432-0800